REMARKS

The above-referenced application is amended to correct additional inadvertant errors identified in the orginally filed specification. No new matter has been added. Entry of this Preliminary Amendment is respectfully requested.

Respectfully submitted,

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MARKED-UP VERSION OF AMENDMENTS

IN THE SPECIFICATION:

1. Please replace the paragraph beginning at page 3, line 24, continuing on to page 4, with the following rewritten paragraph:

--The P^+ diffusion region **122** and the N^+ diffusion region **112** are formed in the N-well region **130**, and a pn junction is formed on a junction face between the P^+ diffusion region **122** and the N-well region **130**. Therefore, a diode can be constituted by using the P^+ diffusion region **122** as an anode and the N^+ diffusion region **112** as a cathode. In the diode element **1000**, one diode includes a junction of a pair of p and n, and therefore as the pn junction area (i.e., the bottom area of the P^+ diffusion region **122**) increases, the current capacity of the diode element **1000** increases. Unlike the N^+ diffusion region **112** or the P^+ diffusion region **122** that have comparatively low electrical resistances, the N-well region **130** has a comparatively high electrical resistance, and thus a parasitic resistance **140** exists in the N-well region **130**. This parasitic resistance **140** is connected in series to the diode constituted by the pn junction between the P^+ diffusion region **122** and the N-well region **130**. Thus, the parasitic resistance **140** of the N-well region **130** causes a voltage drop of the diode. As a result, the current capacity of the diode element **1000** is decreased. Therefore, in order to design the diode element **1000** such that a desired current capacity can be obtained, a layout is designed after determining a P^+ diffusion region size **124** that defines the bottom area of the P^+ diffusion region **122** and a distance (a

distance between the P^+ diffusion region **122** and the N^+ diffusion region **112) 114** that defines the magnitude of the parasitic resistance **[130] 140**.--

2. Please replace the paragraph beginning at page 11, line 16, with the following rewritten paragraph:

--FIGS. **10(a)** to **[10(f)] 10(e)** are cross-sectional views of a process sequence for illustrating a method for producing the diode element **300**.--

3. Please replace the paragraph beginning at page 13, line 16, continuing on to page 14, with the following rewritten paragraph:

--The first unit cell **10** has a first conductive type first semiconductor region **12** formed in the N-well region **30** and a contact region **14** for electrically connecting the first semiconductor region **12** to a line **50**. In this embodiment, the first conductive type first semiconductor region **12** is an N^+ diffusion region, and the N^+ diffusion region **12** is electrically connected to the line **50** through a contact section **52** joined to the contact region **14** provided on the surface thereof. On the other hand, the second unit cell **20** has a second conductive type second semiconductor region **22** formed in the N-well region **30** and a contact region **24** for electrically connecting the [first semiconductor region **10**] second semiconductor region **22** to the line **50**. In this embodiment, the second conductive type second semiconductor region **22** is a P^+ diffusion region, and the P^+ diffusion region **22** is electrically connected to the line **50** through the contact

section **52** joined to the contact region **24** provided on the surface thereof. When a P-well region is formed as a first conductive type semiconductor layer, the first conductive type first semiconductor region **12** can be used as the P^+ diffusion region and the second conductive type second semiconductor region **[12] 22** can be used as the N^+ diffusion region.--

4. Please replace the paragraph beginning at page 19, line 23, continuing on to page 20, with the following rewritten paragraph:

-- Next, as shown in FIG. **2(e)**, after depositing an insulating film **54** on the substrate **60**, contact holes are formed selectively on the insulating film **54**, and then, a line **50** (including contact sections **52**) is formed. Since the contact sections **52** of the line **50** are joined to each of the contact sections **[12] 14** of the first unit cells **10** and the contact sections **[22] 24** of the second unit cells **20**, each of the first unit cells **10** and the second unit cells **20** are electrically connected to the line **50**. Thus, the diode element **100** can be obtained.--

5. Please replace the paragraph beginning at page 26, line 24, with the following rewritten paragraph:

--The diode element **300** can be produced, for example, as shown in FIGS. **10(a)** to **[10(f)] 10(e)**. In this example, a diode element including a gate line **56** that is formed on a gate electrode structure **70** is produced.--

6. Please replace the paragraph beginning at page 27, line 23, with the following rewritten paragraph:

--Next, as shown in FIG. **[10(f)]** **10(e)**, after depositing an insulating film **54** on the SOI substrate, contact holes are formed selectively in the insulating film **54**, and then, a line **50** (including contact sections **52**) and a gate line **56** are formed. Thus, the diode element **300** can be obtained.--